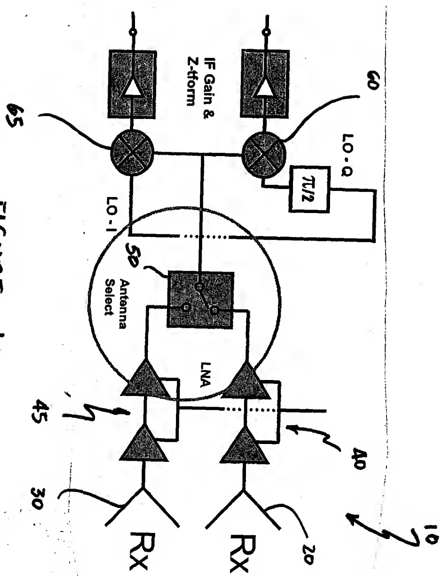


FIGURE 1
-PRIOR ART-

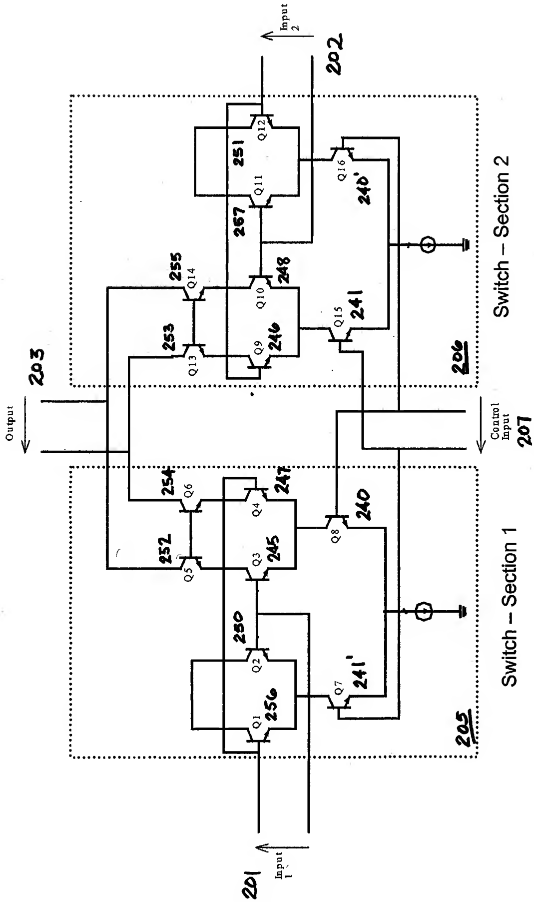
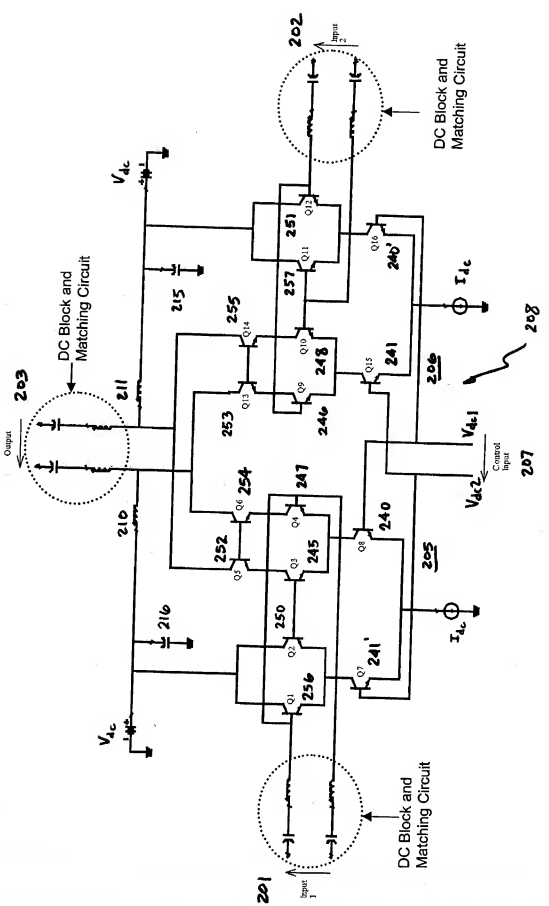

Input 2
202
Output
203
Control Input
207
Input 1
201
Switch – Section 1
Switch – Section 2
205
206
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
240
240'
241
241'
245
246
247
248
250
251
252
253
254
255
256
257

FIGURE 2(a)

FIGURE 2(b)


DC Block and Matching Circuit
DC Block and Matching Circuit
DC Block and Matching Circuit
Input 1
Input 2
Output
Control Input
201
202
203
205
206
207
208
210
211
215
216
240
240'
241
241'
245
246
247
248
250
251
252
253
254
255
256
257
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16

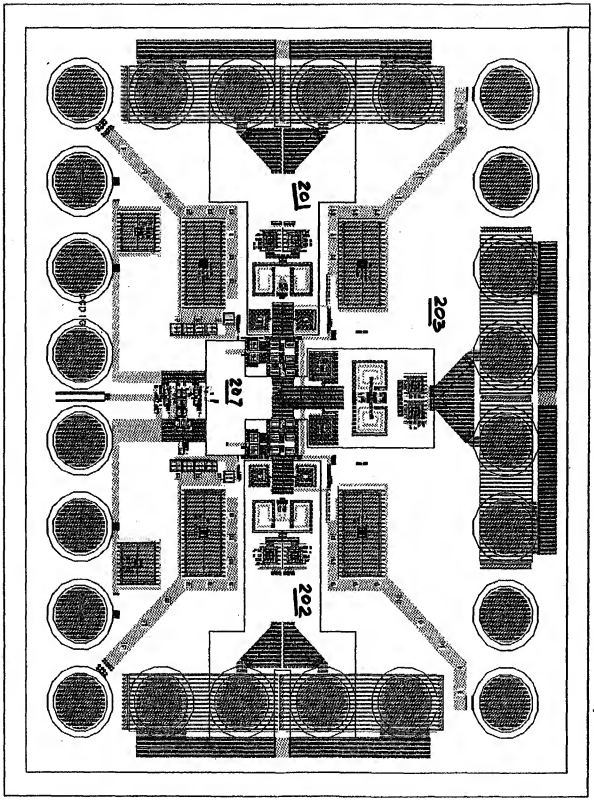


FIGURE 3

FIGURE 4

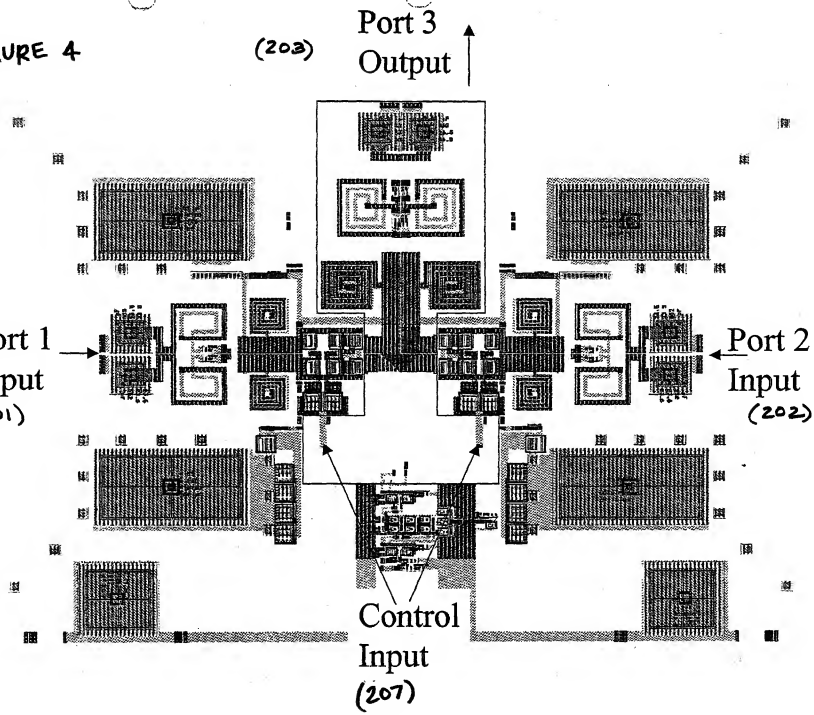

Port 3
Output
(203)
Port 1
Input
(201)
Port 2
Input
(202)
Control
Input
(207)

FIGURE 5(a)
Port 1 - Input Match (Both States)
FIGURE 5(b)
Port 1 - Port 2 Isolation (Both States)
FIGURE 5(c)
Port 1 - Port 3 Isolation (Both States)
FIGURE 5(d)
Port 2 - Input Match (Both States)
FIGURE 5(e)
Port 2 - Port 1 Isolation (Both States)
FIGURE 5(f)
Port 2 - Port 3 Isolation (Both States)
FIGURE 5(g)
Port 1 - Port 3 Transmission (Both States)
FIGURE 5(h)
Port 2 - Port 3 Transmission (Both States)
FIGURE 5(i)
Port 3 - Input Match (Both States)

FIGURE 6

– PRIOR ART –